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12/12/01

J1025 U.S. PTO

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	W2K1070
First Inventor	OH ET AL.
Title	STACKING STRUCTURE OF SEMICONDUCTOR CHIPS AND SEMICONDUCTOR PACKAGE USING IT
Express Mail Label No.	EL 894893805 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☐ Applicant claims small entity status.
See 37 CFR 1.27
3. ☒ Specification [Total Pages]
(preferred arrangement set forth below)
 - Descriptive title of the invention
 - Cross Reference to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to sequence listing, a table, or a computer program listing appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets]
5. Oath or Declaration [Total Pages]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 CFR 1.63 (d))
(for continuation/divisional with Box 17 completed)
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
6. ☐ Application Data Sheet. See 37 CFR 1.76

ADDRESS TO:

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7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - a. ☐ Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ paper
 - c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☒ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☒ Power of Attorney
11. ☐ English Translation Document (if applicable)
12. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
15. ☒ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☐ Other:

J1036 U.S. PTO
10/015374

12/12/01

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:


☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No. _____ / _____
Prior application information Examiner _____ Group / Art Unit _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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Name (Print/Type)	Jeffrey D. Moy	Registration No. (Attorney/Agent)	39,307
Signature		Date	12-11-2001

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT (\$)

1,080.

Complete if Known

Application Number	
Filing Date	
First Named Inventor	OH ET AL.
Examiner Name	
Group Art Unit	
Attorney Docket No	W2K1070

METHOD OF PAYMENT

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number 23-0830

Deposit Account Name WEISS & MOY, P.C.

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status See 37 CFR 1.27

2. ☒ Payment Enclosed:

☒ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
101	740	201	370	Utility filing fee	740
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) (\$) 740

2. EXTRA CLAIM FEES

Total Claims	Extra Claims	Fee from below	Fee Paid
32	-20** = 12	18	216
4	-3** = 1	84	84
Multiple Dependent			-0-

Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$) 300

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

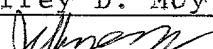
Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for ex parte reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) (\$) 40

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Jeffrey D. Moy	Registration No. (Attorney/Agent)	39,307	Telephone	(480) 994-8888
Signature		Date	12-11-2001		

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Shirley I. Brown

APPLICANT: OH ET AL.

APPLICATION TITLE: STACKING STRUCTURE OF SEMICONDUCTOR
CHIPS AND SEMICONDUCTOR PACKAGE

U.S. SERIAL NUMBER: USING IT

FILING DATE:

TYPE OF INFORMATION ENCLOSED

[X] CHECK NUMBER 09275 FOR \$ 1,080.

[X] DRAWINGS (13 Sheet(s) Enclosed)

[X] NEW PATENT APPLICATION

[] PCT PATENT APPLICATION

[X] OTHER: Certified Copy of Priority Document

STACKING STRUCTURE OF SEMICONDUCTOR CHIPS AND SEMICONDUCTOR PACKAGE USING IT

Kwang Seok Oh
Jong wook Park
Young Kuk Park
Byoung Youl Min

FIELD OF THE INVENTION

The present invention relates to semiconductor chips, and more particularly, to a stacking structure of semiconductor chips and a semiconductor package using it in which a conductive wire can be electrically insulated while a conductive wire is contacted with a lower surface of an upper semiconductor chip thereby preventing mechanical damage of the wire, and also diminishing a total thickness of the stacking structure.

BACKGROUND OF THE INVENTION

As electronic devices get smaller, the components within these devices must get smaller as well. Because of this, there has been an increased demand for the miniaturization of components and greater packaging density. Integrated Circuit (IC) package density is primarily limited by the area available for die mounting and the height of the package. One way of increasing the density is to stack multiple die vertically in an IC package. Stacking multiple die will maximize function and efficiency of the semiconductor package.

In order to stack multiple die vertically in an IC package, an adhesive layer is required between the vertically stacked die. However, presently stacked IC packages require an extraordinarily thick adhesive layer between each die. The thick
5 adhesive layer is necessary in order to prevent the conductive wire of the lower die from contacting the bottom surface of the upper die thereby preventing an electrical short. Unfortunately, the thickness of the adhesive layer limits the number of die that may be vertically stacked in the IC package.

10 Therefore, a need existed to provide a device and method to overcome the above problem.

SUMMARY OF THE INVENTION

15 A semiconductor package and a method of producing the same has a substrate. A first semiconductor chip is coupled to a surface of the substrate. The first semiconductor chip has a first and second surfaces which are substantially flat in nature. An adhesive layer is coupled to the second surface of the first semiconductor chip. A second semiconductor chip having first and
20 second surfaces which are substantially flat in nature is further provided. An insulator is coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds. The second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof.

The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

5 **BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 illustrates a sectional view of one embodiment of the present invention;

FIG. 1A and 1B are magnified views of circle I as shown in FIG. 1;

10 FIG. 2 illustrates a sectional view of another embodiment of the present invention;

FIG. 2A and 2B are magnified views of circle II as shown in FIG. 2;

15 FIG. 3 illustrates a sectional view of another embodiment of the present invention;

FIG. 3A and 3B are magnified views of circle III as shown in FIG.3;

FIG. 4 illustrates a sectional view of another embodiment of the present invention;

20 FIG. 4A is a magnified view of circle IV as shown in FIG.4;

FIG. 5 illustrates a sectional view of another embodiment of the present invention;

25 FIG. 6 illustrates a sectional view of another embodiment of the present invention; and

FIG. 7 illustrates a sectional view of another embodiment of the present invention.

Common reference numerals are used throughout the drawings and detailed description to indicate like elements.

5

DETAILED DESCRIPTION

Referring to FIG. 1, a sectional view of one embodiment of the present invention is shown. FIG.1 illustrates a stacking structure 11 of a semiconductor chip wherein a substrate 7 having a substantially plate form, is provided. As is generally known, a printed circuit board, a circuit tape, a circuit film, a lead frame or the like may be used as the substrate 7. This is only a matter of selection by a person skilled in the art, and, therefore, this does not adversely influence the present invention.

As shown in FIG. 1, a first semiconductor chip 1 is bonded on a top surface of the substrate 7. The semiconductor chip 1 includes a first surface 1a and a second surface 1b, which are substantially flat in nature. A plurality of input-output pads 1c are formed on the second surface 1b of the first semiconductor chip 1.

There is an edge pad type semiconductor chip 1 in which a plurality of input-output pads 1c are formed at the inner circumference of the second surface 1b. A center pad type semiconductor chip will be described with reference to FIG. 4 hereafter.

An adhesive layer 3 having a predetermined thickness is bonded on the inside of the second surface 1b of the first semiconductor chip 1, excluding the input-output pads 1c. The adhesive layer 3 may include such substances as a nonconductive liquid phase adhesive, a nonconductive adhesive tape or other substances that are commonly known in the art for semiconductor chip attachment.

The adhesive layer 3 serves as an adhesive bonding to the second semiconductor chip 2 on the second surface 1b of the first semiconductor chip 1. Here, it is possible for the adhesive layer 3 to be formed in the same thickness as a loop height of a first conductive wires 5 mentioned below or a smaller thickness than the loop height. However, when the thickness of the adhesive layer 3 is thinner than the loop height, it is desirable that the thickness of the adhesive layer 3 is to be more than about 80% of the loop height. This will be described in detail hereafter.

Continuously, the input-output pads 1c of the first semiconductor chip 1 and the substrate 7 can be bonded to each other by the first conductive wires 5, such as gold or copper or aluminum wires or by its equivalent. This is performed by a conventional normal wire bonding manner which will be described hereafter. It should be noted that the listing of the different types of wires is just used as an example and should not be seen as to limit the scope of the present invention.

Continuously, a second semiconductor chip 2 having a first surface 2a and a second surface 2b, which are substantially flat in nature, is placed on the upper part of the adhesive layer 3. A plurality of input-output pads 2c are formed on the second surface 2b of the second semiconductor chip 2.

An insulator 4 is formed on the first surface 2a of the second semiconductor chip 2. That is, the insulator 4 formed on the first surface 2a of the second semiconductor chip 2 is bonded on the upper part of the adhesive layer 3.

The insulator 4 may include such substances as a liquid phase adhesive, an adhesive tape/film, a polyimide, an oxide layer and a nitride layer or other substances that are commonly known in the art for semiconductor chip or package. It is desirable that all these insulators have a nonconductive, soft, and elastic nature. Also, it is desirable that the thickness of the insulator 4 may be more than about 20% of the loop height of the first conductive wires 5.

The insulator 4, but not limited to, is formed in a wafer state before separating into individual semiconductor chips. That is, the insulator 4 can be formed by bonding the nonconductive tape/film on the back surface of the wafer, or by coating the nonconductive liquid phase adhesive or the polyimide on the back surface of the wafer in a spin coating or in a spray manner. Also, the insulator 4 can be formed by evaporating a relatively thicker oxide layer or nitride layer on the back surface of the wafer.

After forming the nonconductive tape/film, nonconductive liquid phase adhesive, polyimide, oxide layer or nitride layer (insulator) on the back surface of the wafer, a plurality of semiconductor chips are separated from the wafer, respectively.

Alternatively, insulator 4 may be formed at the individual semiconductor chip which is already separated from the wafer. Namely, after the semiconductor chip is separated from the wafer, the insulator 4 is formed at back surface of the semiconductor chip as described above.

As mentioned above, after forming insulator 4 on the first surface 2a of the second semiconductor chip 2, the second chip 2 is compressed and adhered to the upper part of adhesive layer 4.

At this time, since thickness of the adhesive layer 3 may be about the same or thinner than the loop height of the first conductive wires 5, the first conductive wires 5 may be contacted with the insulator 4 formed at the first surface 2a of the second semiconductor chip 2. However, the loop height portion of the first conductive wires 5 exposed outward from adhesive layer 3 is about 20% of total loop height in the first conductive wires 5. And thickness of the insulator 4 is more than 20% of the total loop height of the first conductive wires 5. Thus, the first conductive wires 5 do not directly contact to the first surface 2a of the second semiconductor chip 2.

Even in the case that the loop height portion of the first conductive wires 5 become exposed outward from adhesive layer 3, the first conductive wires 5 do not directly contact to the first surface 2a of the second semiconductor chip 2 by the insulator 4. Also, since the insulator 4 has a nonconductive, soft, and elastic nature, the first conductive wires 5 have no electrical or mechanical damages. Namely, the first conductive wires 5 can be easily overlapped or superimposed with the insulator 4 and the conductive wires 5 can be independent in the insulator 4. Thus, the first conductive wires 5 do not short each other and aren't heavily damaged by the insulator 4. The tape/film as the insulator 4 seems to have the most soft and elastic nature among the insulator mentioned above.

An edge pad type semiconductor chip 2, in which a plurality of input-output pads 2c is formed at the inner circumference of the second surface 2b, is illustrated in the FIG. 1. However, a center pad type semiconductor chip 2, in which a plurality of input-output pads 2c is formed at the center of the second surface 2b, can also be used.

Continuously, the input-output pads 2c of the second semiconductor chip 2 and the substrate 7 can be bonded to each other by the second conductive wires 6, as described above or its equivalent.

As shown in FIG. 1A and 1B, which is a magnified view of circle I as shown in FIG. 1, the above conventional normal wire bonding is constructed in such a manner that an end of the

conductive wire 5 is bonded on the input-output pad 1c of the semiconductor chip 1 by conductive ball 51(ball bonding). Then the other end of the conductive wire 5 is bonded on the substrate 7 by stitch bonding.

5 As shown in FIG. 1A, if the adhesive layer 3 does not cover the input-output pads 1c, the wire bonding can be performed selectively before or after formation of the adhesive layer 3.

10 However, as shown in FIG. 1B, if adhesive layer 3 covers the input-output pads 1c, then the wire bonding must be performed before forming the adhesive layer 3. Here, if the adhesive layer 3 covers the input-output pads 1c of the semiconductor chip 1, the nonconductive liquid phase adhesive as adhesive layer 3 is generally used. That is, the adhesive tape as adhesive layer 3 may affect damages in the first conductive wires 5.

15 According to the stacking structure 11 of the present invention, the first conductive wires 5 are not directly contacted with the first surface 2a of the semiconductor chip 2. Thus, the phenomenon of an electrical short will not occur. Furthermore, mechanical damage of the first conductive wires 5 can also be prevented. Though the first conductive wires 5 are contacted with the insulator 4, electrical or mechanical damage has never occurred. That is, because of a nonconductive, soft and elastic nature of insulator 4, the first conductive wires 5 can be easily overlapped or superimposed with the insulator 4 and the conductive wires 5 can be independent in the insulator 4. Thus, the first conductive wires 5 do not short each other and aren't heavily

damaged by the insulator 4.

Also, the thickness of the adhesive layer 3 can adequately become thinner. Namely, in prior art, the adhesive layer 3 should be formed in substantially twice the thickness of the loop height of the first conductive wires 5. However, in the present the invention, the adhesive layer 3 can be formed in the same thickness as the loop height of the first conductive wires 5 or a thickness that is less than the loop height. Thus, this invention can diminish a total thickness of the stacking structure of the semiconductor chips.

Referring to FIG. 2, a sectional view of another embodiment of the present invention is illustrated. Referring also to FIG. 2A and 2B, magnified views of circle II shown in FIG. 2 are also illustrated. Since a stacking structure 12 illustrated in FIG. 2 is constructed in a similar manner to the stacking structure of FIG. 1, only differences existing there between will be described herein below.

As shown in FIG. 2 or FIG. 2A, the first and the second conductive wires 5 and 6 are not formed from a conventional normal bonding manner. Instead, a reverse bonding manner is used. Namely, the conventional normal bonding is constructed in such a manner that an end of the conductive wire is bonded on the input-output pad of the semiconductor chip by ball bonding. The other end of the conductive wire is then bonded on the substrate by stitch bonding.

Meanwhile, the reverse bonding is constructed in such a manner that an end of the conductive wire 5 is bonded on the substrate by conductive ball 51' (ball bonding). Then the other end of the conductive wire 5 is bonded on the input-output pad 1c of the semiconductor chip 1 by stitch bonding. Of course, a conductive ball 51 is formed on the input-output pads of semiconductor chip 1 by the conductive wire 5 in advance in order to alleviate an impulse created by the stitch bonding. The reverse bonding can be applied to all the first and second conductive wires 5 and 6 by which the first semiconductor chip 1 and the second semiconductor chip 2 are connected to the substrate 7, respectively.

In the case where the reverse bonding is used, the thickness of the adhesive layer 3 can be thinner owing to a lower loop height of the first conductive wires 5. That is, as the loop height of the conductive wire 5, which is bonded by the stitch bonding, is very low, the thickness of the adhesive layer 3 can be reduced sharply.

Also, since the loop height of the conductive wires 5 is low, when the second semiconductor chip 2 is adhered or compressed to the adhesive layer 3, the first conductive wires 5 have less mechanical stress than the first embodiment. Thus, the first conductive wires 5 can not create an electrical short or mechanical damage.

In certain cases, the insulator 4 having elevated bonding power can be used as bonding materials without using the adhesive layer 3. Nevertheless, since the insulator 4 has the nonconductive, soft and elastic nature, the first conductive wires 5 can not create an electrical short or mechanical damage.

Of course, the adhesive layer 3 may cover the input-output pads 1c of the first semiconductor chip 1 (not shown) and the second conductive wires 6 may connect between the input-output pads 2c and the substrate 7 by normal bonding.

Further, as shown in FIG.2B, a wedge bonding manner can be applied to the first and the second conductive wires 5 and 6 in order to lower the loop height. That is, the wedge bonding is constructed in such a manner that an end of the conductive wire is bonded on the input-output pad of the semiconductor chip by stitch bonding. Then, the other end of the conductive wire is bonded on the substrate by stitch bonding.

Similarly, in the case where the wedge bonding is used, the thickness of the adhesive layer 3 can be thinner owing to a lower loop height of the first conductive wires 5. That is, as the loop height of the conductive wire, which is bonded by the stitch bonding, is very low, the thickness of the adhesive layer 3 can be reduced sharply.

Also, since the loop height of the conductive wires 5 is low, when the second semiconductor chip 2 is adhered or compressed to the adhesive layer 3, the first conductive wires 5 have less mechanical stress than the first embodiment.

Referring to FIG. 3, a sectional view of another embodiment of the present invention is illustrated. Also referring to FIG. 3A and 3B, magnified views of circle III as shown in FIG. 3 are illustrated. Since a stacking structure 13 is constructed in a similar manner to the stacking structure 12 of FIG. 2, only differences existing there between will be described herein below. As shown in FIG. 3 and 3A, the first and the second conductive wires 5 and 6 are formed by a reverse bonding manner. The conductive ball 51 is formed on the input-output pads 1c and 2c of the semiconductor chip 1 and 2 by the conductive wire in advance in order to alleviate an impulse created by the stitch bonding.

Furthermore, a supporter 52 is formed on the upper part of the conductive wires 5 connected with input-output pads 1c of the semiconductor chip 1. Namely, the supporter 52 is formed on the upper part of the conductive balls 51 and the first conductive wires 5 together. Also, the supporter 52 may be formed on the outside of the input-output pads 1c. For example, a plurality of the supporters 52 can be formed on the inner circumference of the second surface 1b of the semiconductor chip 1.

The supporter 52 may be formed after wire bonding. Namely, first of all, the conductive ball 51 is formed on the input-output pads 1c, and the first conductive wire 5 is bonded to the conductive ball 51. At last, the supporter 52 is formed on the first conductive wire 5 superimposed over the conductive ball 51.

The supporter 52 may be formed by conventional stud bump forming manner. For example, a ball is formed at end of a conductive wire, and the ball is fused to the top of the first conductive wire 5. The conductive wire is then cut off except the ball. Furthermore, another ball is formed at the end of the conductive wire, and this ball is bonded to the fused ball above mentioned. As for a repetition of this manner, as shown in FIG. 3A, a raw type conductive ball forms the supporter 52.

The supporter 52 may include such substances as gold, silver, copper, and solder or other substances that are commonly known in the art for the semiconductor chip. The above listing of substances should not be seen as to limit the scope of the present invention.

Meanwhile, the supporter 52 is contacted with the bottom of the insulator 4 formed on the second semiconductor chip 2 so as to support the second semiconductor chip 2. Thus, since the supporter 52 supports many portions of the insulator 4 formed on the semiconductor chip 2, the semiconductor chip 2 will be supported more stable. Of course, the adhesive layer 3 may cover the input-output pads 1c of the first semiconductor chip 1 and the supporter 52.

Further, as shown in FIG.3B, a wedge bonding manner can be applied to the first and the second conductive wires 5 and 6 in order to lower the loop height.

Similarly, the supporter 52 is formed on the upper part of the conductive wires 5 connected with input-output pads 1c of the semiconductor chip 1. The supporter 52 is contacted with the insulator 4 so as to support the second semiconductor chip 2. Thus, since the supporter 52 supports the insulator 4 formed on the semiconductor chip 2, the semiconductor chip 2 becomes more stable.

Also, since the conductive wires 5 is covered with supporter 52, when the second semiconductor chip 2 is adhered or compressed to the adhesive layer 3, the first conductive wires 5 have less mechanical stress than the previous embodiments.

Referring to FIG. 4, a sectional view of another embodiment of the present invention is illustrated. And referring to FIG. 4A, magnified views of circle IV as shown in FIG. 4 is illustrated. Since a stacking structure 14 is constructed in a similar manner to the stacking structure 12 of FIG. 2, only differences existing there between will be described herein below.

As shown in the drawings, there is a center pad type semiconductor chip 1 in which a plurality of input-output pads 1c are formed at the center of the second surface 1b. Also, the input-output pads 1c of the first semiconductor chip 1 and the substrate 7 are bonded to each other by the reverse bonding of the first conductive wires 5.

The reverse bonding manner, as described above, has advantages in that the thickness of the adhesive layer 3 can be thinner. Furthermore, the first conductive wires 5 don't make

contact with the region except for the input-output pads 1c of the first semiconductor chip 1 without increasing the loop height.

Here, it is, but not limited to, that a nonconductive liquid phase adhesive is used as the adhesive layer 3. That is, as a certain portion of the first conductive wires 5 is positioned at the inside of the adhesive layer 3, it is desirable to use the nonconductive liquid phase adhesive rather than solid phase adhesive tape. In other words, the input-output pads 1c of the first semiconductor chip 1 and the substrate 7 is bonded to each other by the reverse bonding of the first conductive wires 5. Of course, conductive balls 51 are formed on the input-output pads 1c of the semiconductor chip 1 by the conductive wire in advance in order to alleviate an impulse created by the stitch bonding.

The nonconductive liquid phase adhesive is applied to the first surface 1a of the first semiconductor chip 1 and is hardened. Then, the second semiconductor chip 2, to which the insulator 4 is stuck, is bonded on the adhesive layer 3. The insulator 4 may include such substances as a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer and a nitride layer or other substances that are commonly known in the art for semiconductor chips or packages, as described above. Again, the listing of the above substances should not be seen as to limit the scope of the present invention.

Further, a wedge bonding can be applied to the first and the second conductive wires 5 and 6 in order to lower the loop

height. That is, the wedge bonding is constructed in such a manner that an end of the conductive wire is bonded on the substrate by stitch bonding. Then, the other end of the conductive wire is bonded on the input-output pad of the semiconductor chip by stitch bonding.

Also, in the FIG. 4, the input-output pads 2c of the second semiconductor chip 2 are bonded to substrate 7 by the reverse bonding of conductive wires 6. However, the normal bonding manner is also possible. Furthermore, the second semiconductor chip 2 of the edge pad type is illustrated in FIG. 4. However, the center pad type is also possible. In this case, the second conductive wires 6 are generally bonded to substrate 7 by the reverse bonding or wedge bonding.

Meanwhile, the stacking structures according to the present invention are described on the basis of the first and the second semiconductor chips 1 and 2. However, a plurality of semiconductor chips (for example, a third semiconductor chip, a fourth semiconductor chip, etc.) may be stacked one up on another. It will be appreciated by those persons skilled in the art that such an arrangement is optional. In other words, the present invention is not limited by a number of the stacked semiconductor chips.

Referring to FIG. 5, a sectional view of another embodiment of the present invention is illustrated. The stacking structure of the semiconductor chip is identical with that of FIG.

1. As shown in the FIG. 5, a substrate 70 having a substantially plate form is provided. The substrate 70 includes resin layer 71, a plurality of circuit patterns 72 formed at a top and bottom of the resin layer 71 and a plurality of conductive via 73 connecting the top and bottom circuit patterns 72. The substrate 70, as is generally known, may be a printed circuit board, circuit tape or circuit film. The listing of the substrates 70 should not be seen as to limit the scope of the present invention.

A first semiconductor chip 1 is bonded on a surface of the substrate 70. The semiconductor chip 1 includes a first surface 1a and a second surface 1b, which are substantially in a flat type. A plurality of input-output pads 1c are formed on the second surface 1b of the first semiconductor chip 1.

The input-output pads 1c of the first semiconductor chip 1 and some top circuit patterns 72 of the substrate 70 are bonded to each other by the first conductive wires 5.

An adhesive layer 3 having a predetermined thickness is bonded on the second surface 1b of the first semiconductor chip 1.

A second semiconductor chip 2 having a first surface 2a and a second surface 2b, which are substantially in a flat type, is positioned on the upper part of the adhesive layer 3. A plurality of input-output pads 2c are formed on the second surface 2b of the second semiconductor chip 2. Further, an insulator 4 is formed on the first surface 2a of the second semiconductor chip 2. The input-output pads 2c of the second semiconductor chip 2 and others

top circuit patterns 72 of the substrate 70 are bonded to each other by the second conductive wires 6.

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Moreover, the first semiconductor chip 1, the adhesive layer 3, the second semiconductor chip 2, insulator 4, the first and the second conductive wires 5 and 6 are sealed with sealing material, such as an epoxy molding compound. The area sealed with the sealing material is defined as a sealing part 8.

Finally, conductive balls 9 such as solder balls are fused to the bottom circuit patterns of the substrate 70. Such semiconductor package 15 can be mounted to a mother board later.

Referring to FIG. 6, a sectional view of another embodiment of the present invention is illustrated. The stacking structure of the semiconductor chip is identical with that of FIG. 1. Since the semiconductor package 16 is constructed in a similar manner to the semiconductor package 15 of FIG. 5, only differences existing there between will be described herein below.

As shown in FIG. 6, a perforating hole 74 of which size is larger than that of the semiconductor chip 1 is formed on a center of the substrate 70. A plurality of circuit patterns 72 are formed at the outside of the perforating hole 74. The semiconductor chip 1 is located in the perforating hole 75 so as to form a thinner semiconductor package 15. The input-output pads 1c of the semiconductor chip 1 are bonded to circuit patterns 72 by the first conductive wires 5.

Furthermore, the sealing part 8 is formed inside at the perforating hole 74, and the first surface 1a of the semiconductor chip 1 is exposed outward from the sealing part 8 so as to increase

the heat dissipation capability of the first semiconductor chip 1.

Since the semiconductor chip and the substrate is overlapped by each other, the total thickness of the semiconductor package 15 becomes thinner. Furthermore, since the first surface 1a of the semiconductor chip 1 is exposed outward from the sealing part 8, the semiconductor package 15 increases its heat dissipation capability.

Referring to FIG. 7, a sectional view of another embodiment of the present invention is illustrated. A stacking structure of the semiconductor chip is identical with that of FIG. 1. As shown in FIG. 7, a substrate 80 having a substantially plate form is provided. The substrate 80 includes chip mounting plate 81 and a plurality of leads 82 formed at an outside of the chip mounting plate 81. Such a substrate 80, as is generally known, may be a conventional lead frame or a micro lead frame (MLF).

A first semiconductor chip 1 is bonded to the chip mounting plate 81 of the substrate 80. The semiconductor chip 1 includes a first surface 1a and a second surface 1b, which are substantially flat in nature. A plurality of input-output pads 1c are formed on the second surface 1b of the first semiconductor chip 1. The input-output pads 1c of the first semiconductor chip 1 and some leads 82 of the substrate 80 are bonded to each other by the first conductive wires 5.

An adhesive layer 3 having a predetermined thickness is bonded on the second surface 1b of the first semiconductor chip 1.

5 A second semiconductor chip 2 having a first surface 2a and a second surface 2b, which are substantially flat in nature, is positioned on the upper part of the adhesive layer 3. A plurality of input-output pads 2c are formed on the second surface 2b of the second semiconductor chip 2. An insulator 4 is formed on the first surface 2a of the second semiconductor chip 2.

The input-output pads 2c of the second semiconductor chip 2 and others leads 82 of the substrate 80 are bonded to each other by the second conductive wires 6.

10 Moreover, the first semiconductor chip 1, the adhesive layer 3, the second semiconductor chip 2, insulator 4, the first and the second conductive wires 5 and 6, and the substrate 80 are sealed with sealing material, such as an epoxy molding compound. The area sealed with the sealing material is defined as a sealing part 8. Here, a bottom surface of the chip mounting plate 81 and plurality of leads 82 are exposed outward from the sealing part 8.

15 Also, these semiconductor packages 15, 16 and 17 can include the stacking structures illustrated in FIG. 2, 3 and 4. Furthermore, the stacking structure according to the present invention is described on the basis of the first and the second semiconductor chips 1 and 2. However, a plurality of semiconductor chips (for example, a third semiconductor chip, a fourth semiconductor chip, etc.) may be stacked one up on another. It will be appreciated by those persons skilled in the art that such an arrangement is optional. In other words, the present invention

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is not limited by the number of the semiconductor chip.

According to the stacking structure of the semiconductor chip and the semiconductor package using it, the insulator is further formed on the first surface of the second semiconductor chip, where it can be electrically insulated while the conductive wire is contacted with the insulator.

Also, the insulator is made from a soft or elastic material, thereby preventing the mechanical damage of the conductive wire. Furthermore, the thickness of the adhesive layer can become thinner adequately in order to diminish a total thickness of the stacked semiconductor chip or package.

Moreover, the conductive wire is stuck to the insulator, thereby having the effect of preventing the leaning phenomenon of the conductive wire during the sealing process and or the like.

This disclosure provides exemplary embodiments of the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material and manufacturing process may be implemented by one of skill in the art in view of this disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a substrate;

5 a first semiconductor chip coupled to a surface of the substrate, the first semiconductor chip having first and second surfaces which are substantially flat in nature;

an adhesive layer coupled to the second surface of the first semiconductor chip;

10 a second semiconductor chip having first and second surfaces which are substantially flat in nature; and

15 an insulator coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof.

2. A semiconductor package in accordance with Claim 1 further comprising:

at least one input-output pad being formed on the second surface of the first semiconductor chip; and

20 at least one first conductive wire connecting the input-output pad of the first semiconductor chip and the substrate.

3. A semiconductor package in accordance with Claim 2 further comprising:

at least one input-output pads formed on the second surface of the second semiconductor chip; and

5 at least one second conductive wire connecting the input-output pads of the second semiconductor chip and the substrate.

4. A semiconductor package in accordance with Claim 3 wherein the first semiconductor chip is an edge pad type semiconductor chip in which the input-output pad of the first semiconductor chip is formed at an inner circumference of the second surface.

10 15 5. A semiconductor package in accordance with Claim 3 wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

20 6. A semiconductor package in accordance with Claim 3 wherein the adhesive layer covers a part of the first conductive wire positioned on the input-output pad of the first semiconductor chip.

7. A semiconductor package in accordance with Claim 3 wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

8. A semiconductor package in accordance with Claim 3 wherein a first end of the first conductive wire is bonded on the substrate by ball bonding and a second end of the first conductive wire is bonded on the input-output pad of the first semiconductor chip by stitch bonding.

9. A semiconductor package in accordance with Claim 8 wherein a conductive ball is formed on the input-output pad of the first semiconductor chip bonded by the stitch bonding.

10. A semiconductor package in accordance with Claim 8 further comprising a supporter formed on the first conductive wire connected on the input-output pad so as to support the second semiconductor chip.

11. A semiconductor package in accordance with Claim 3 wherein the first semiconductor chip is a center pad type semiconductor chip in which the input-output pad is formed at the center of the second surface thereof.

12. A semiconductor package in accordance with Claim 3 wherein a first end of the first conductive wire is bonded on the substrate and a second end of the first conductive wire is bonded on the input-output pad of the first semiconductor chip by stitch bonding.

13. A semiconductor package in accordance with Claim 11 wherein a first end of the first conductive wire is bonded on the substrate and a second end of the first conductive wire is bonded on the input-output pad of the first semiconductor chip by stitch bonding.

14. A semiconductor package in accordance with Claim 11 wherein the adhesive layer is a nonconductive liquid phase adhesive.

15. A semiconductor package in accordance with Claim 11 wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

16. A semiconductor package in accordance with Claim 3 wherein a section of the first conductive wires is contacted with the insulator.

17. A semiconductor package comprising:

a substrate on which a plurality of circuit patterns is formed;

a first semiconductor chip having first and second surfaces wherein the first surface of the first semiconductor chip is coupled to the substrate,

a plurality of input-output pads formed on the second surface of the first semiconductor chip;

an adhesive layer coupled to the second surface of the first semiconductor chip;

a second semiconductor chip having first and second surfaces;

an insulator coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof;

a plurality of input-output pads formed on the second surface thereof;

a plurality of first conductive wires connecting the input-output pads of the first semiconductor chip and the circuit pattern of the substrate;

a plurality of second conductive wires connecting the input-output pads of the second semiconductor chip and the circuit pattern of the substrate; and

18. A semiconductor package in accordance with Claim 17 wherein the substrate is one selected from a group consisting of a printed circuit board, a circuit tape, a circuit film, a lead frame, and combinations thereof.

5

19. A semiconductor package in accordance with Claim 17 further comprising a conductive ball coupled to a surface of the substrate.

10

20. A semiconductor package in accordance with Claim 17 wherein the substrate has a perforating hole of which size is larger than that of the first semiconductor chip.

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21. A semiconductor package comprising:

a substrate;

a first semiconductor chip coupled to a surface of the substrate, the first semiconductor chip having first and second surfaces which are substantially flat in nature;

an adhesive layer coupled to the second surface of the first semiconductor chip; and

a second semiconductor chip having first and second surfaces which are substantially flat in nature; and

means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the means for preventing shorting of wirebonds.

22. A semiconductor package in accordance with Claim 21 further comprising:

at least one input-output pad being formed on the second surface of the first semiconductor chip;

at least one first conductive wire connecting the input-output pad of the first semiconductor chip and the substrate;

at least one input-output pads formed on the second surface of the second semiconductor chip; and

at least one second conductive wire connecting the input-output pads of the second semiconductor chip and the substrate.

23. A method of forming a semiconductor package comprising:

providing a substrate;

5 coupling a first semiconductor chip to a surface of the substrate, the first semiconductor chip having first and second surfaces which are substantially flat in nature;

laying an adhesive layer to the second surface of the first semiconductor chip; and

10 providing a second semiconductor chip having first and second surfaces which are substantially flat in nature; and

forming an insulator coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof.

15 24. The method of Claim 23 further comprising:

forming at least one input-output pad on the second surface of the first semiconductor chip; and

20 coupling at least one first conductive wire from the input-output pad of the first semiconductor chip to the substrate.

25. The method of Claim 23 further comprising:

forming at least one input-output pads on the second surface of the second semiconductor chip; and

connecting at least one second conductive wire from the input-output pads of the second semiconductor chip to the substrate.

26. The method of Claim 23 further comprising:

providing an edge pad type semiconductor chip as the first semiconductor chip; and

forming the input-output pad of the first semiconductor chip at an inner circumference of the second surface.

27. The method of Claim 23 further comprising:

ball bonding a first end of the first conductive wire to the substrate; and

stitch bonding a second end of the first conductive wire to the input-output pad of the first semiconductor chip.

28. The method of Claim 27 further comprising forming a conductive ball on the input-output pad of the first semiconductor chip bonded by the stitch bonding.

29. The method of Claim 27 further comprising forming a supporter on the first conductive wire connected on the input-output pad so as to support the second semiconductor chip.

5 30. The method of Claim 23 further comprising:

providing a center pad type semiconductor chip as the first semiconductor chip; and

forming the input-output pad at a center of the second surface thereof.

10 31. The method of Claim 23 further comprising:

bonding a first end of the first conductive wire to the substrate; and

15 stitch bonding a second end of the first conductive wire to the input-output pad of the first semiconductor chip.

32. The method of Claim 30 further comprising:

bonding a first end of the first conductive wire to the substrate; and

20 stitch bonding a second end of the first conductive wire to the input-output pad of the first semiconductor chip.

ABSTRACT OF THE INVENTION

A semiconductor package and a method of producing the same has a substrate. A first semiconductor chip is coupled to a surface of the substrate. The first semiconductor chip has a first and second surfaces which are substantially flat in nature. An adhesive layer is coupled to the second surface of the first semiconductor chip. A second semiconductor chip having first and second surfaces which are substantially flat in nature is further provided. An insulator is coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds. The second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof.

FOR THE RECORD

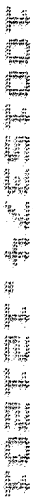


FIG. 1A

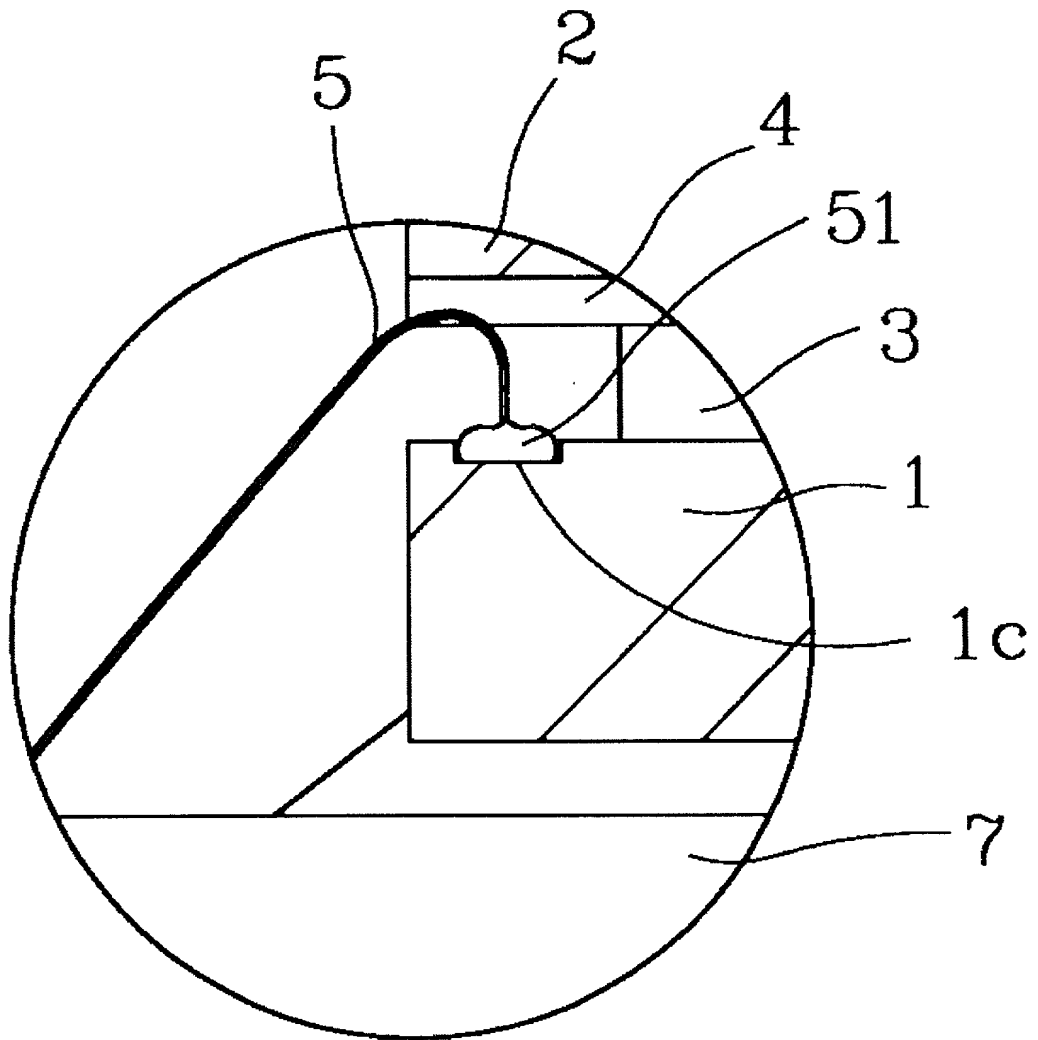


FIG. 1B

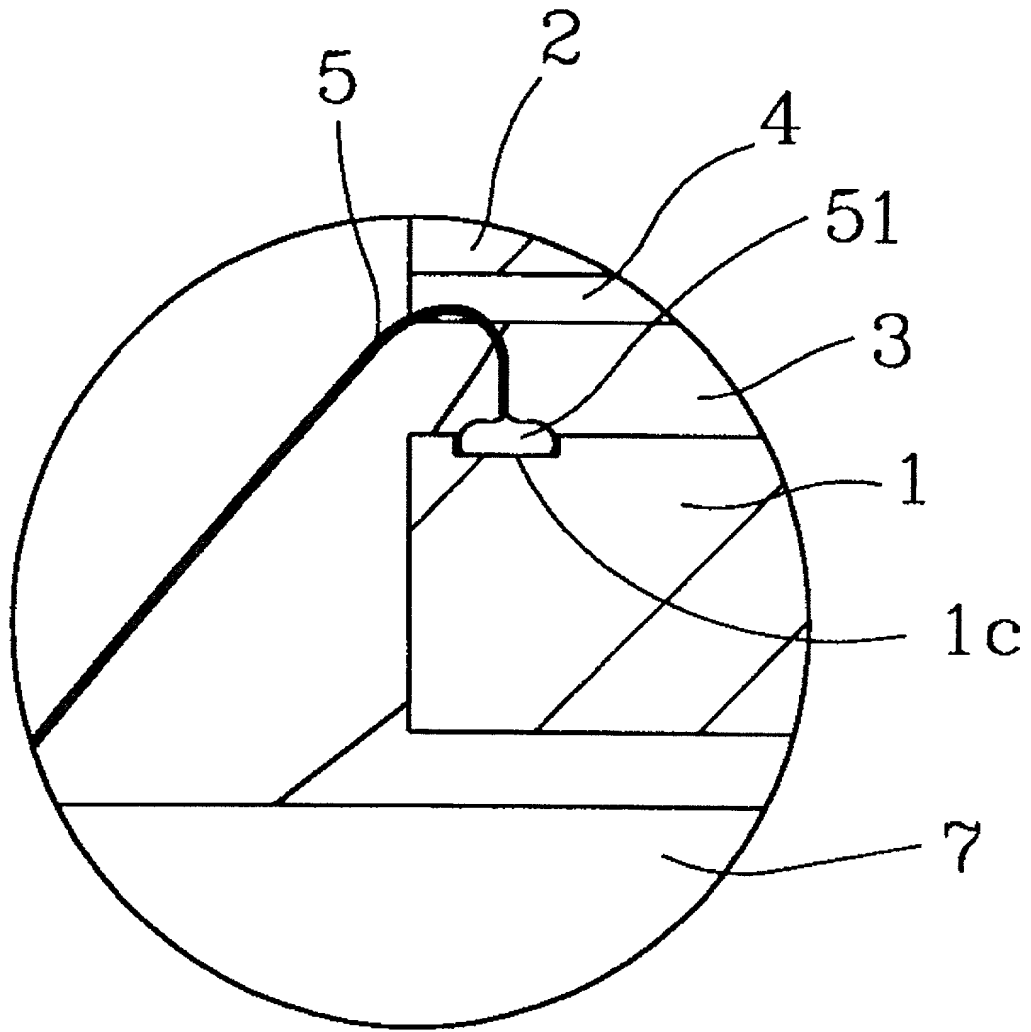


FIG. 2

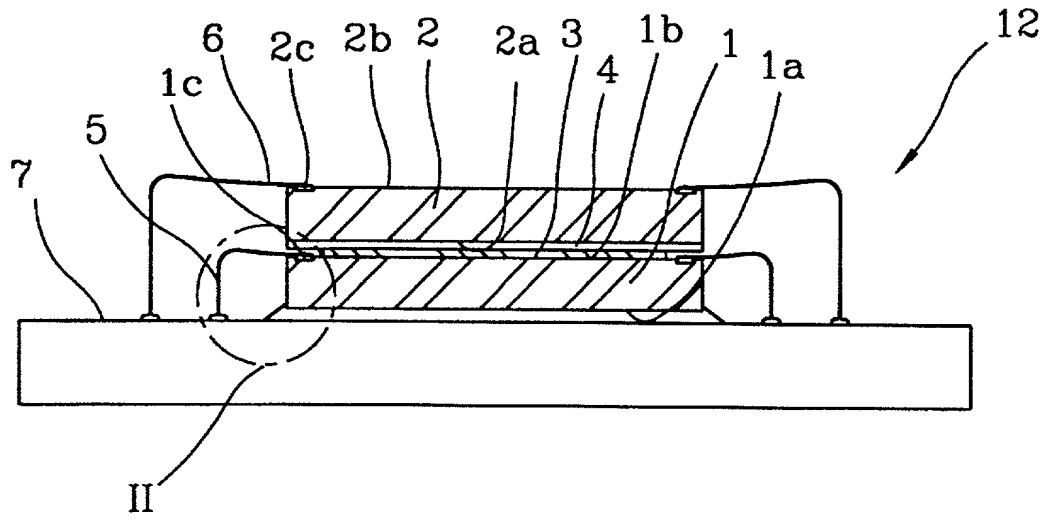


FIG. 2A

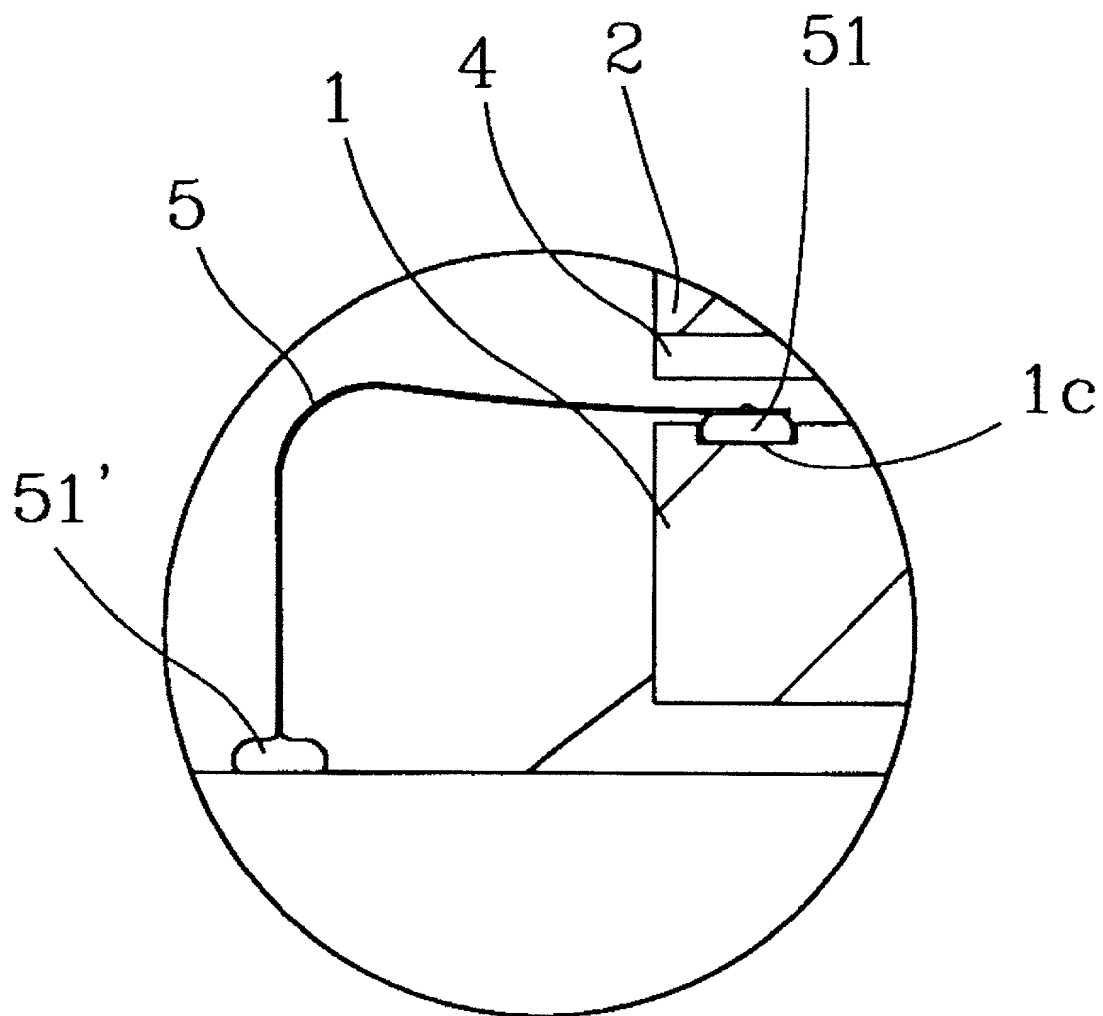


FIG. 2B

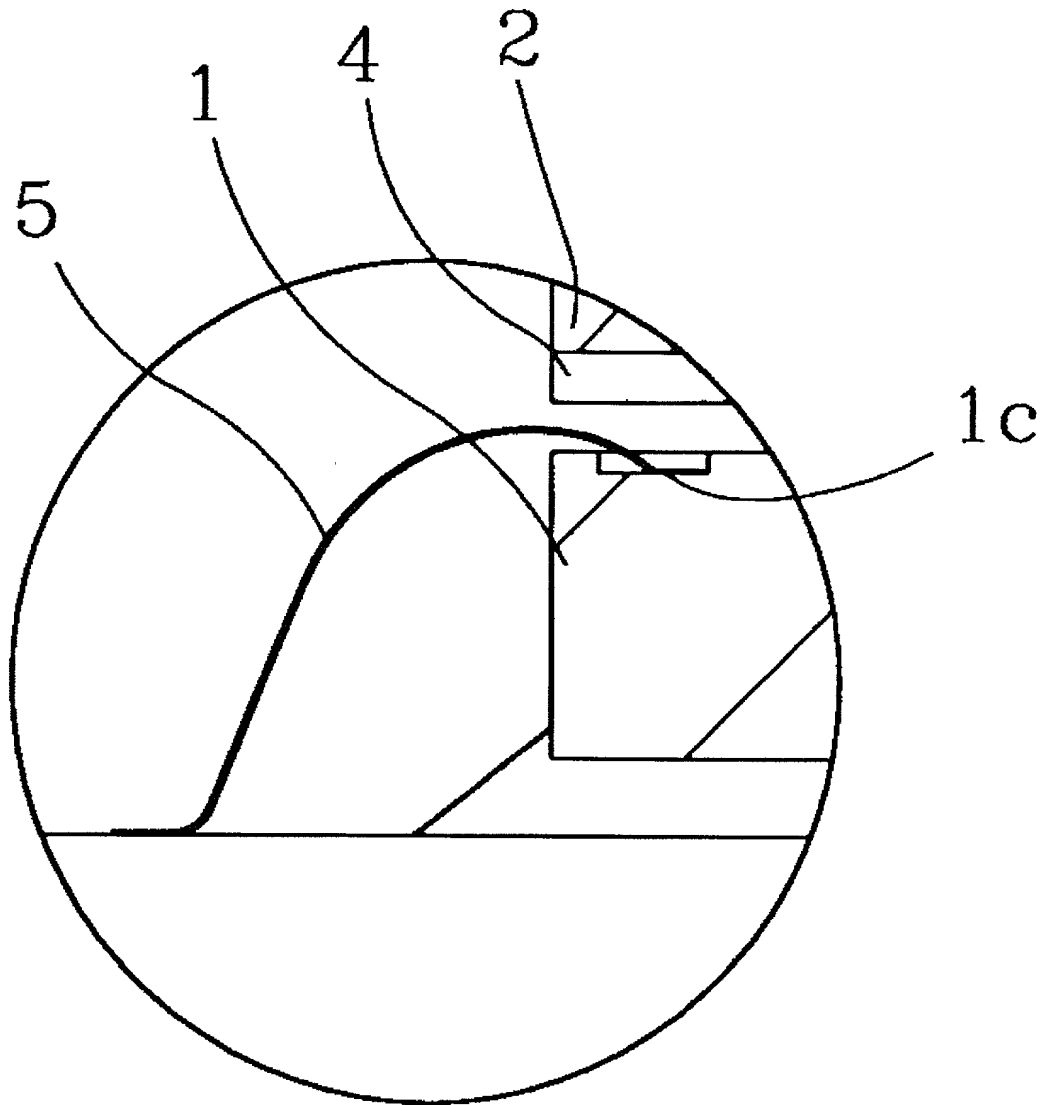


FIG. 3

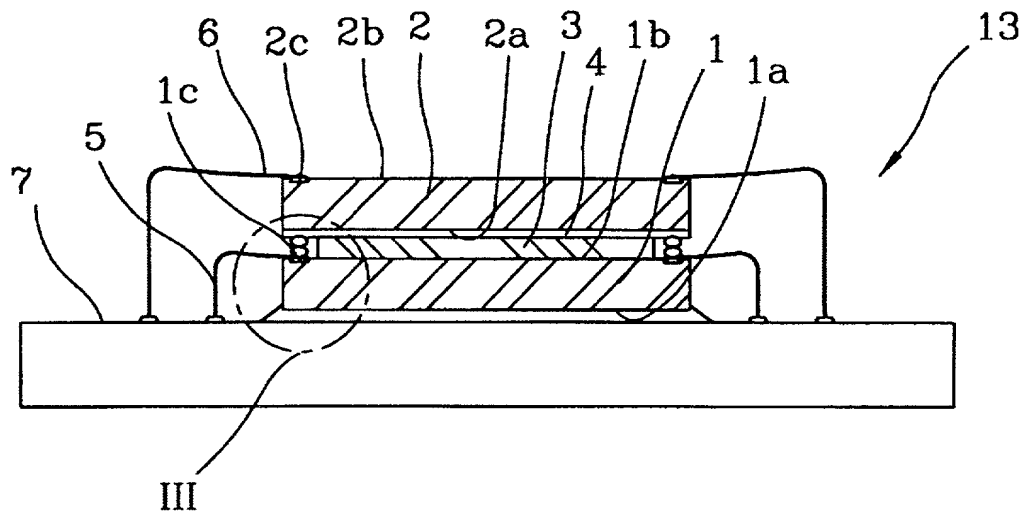


FIG. 3A

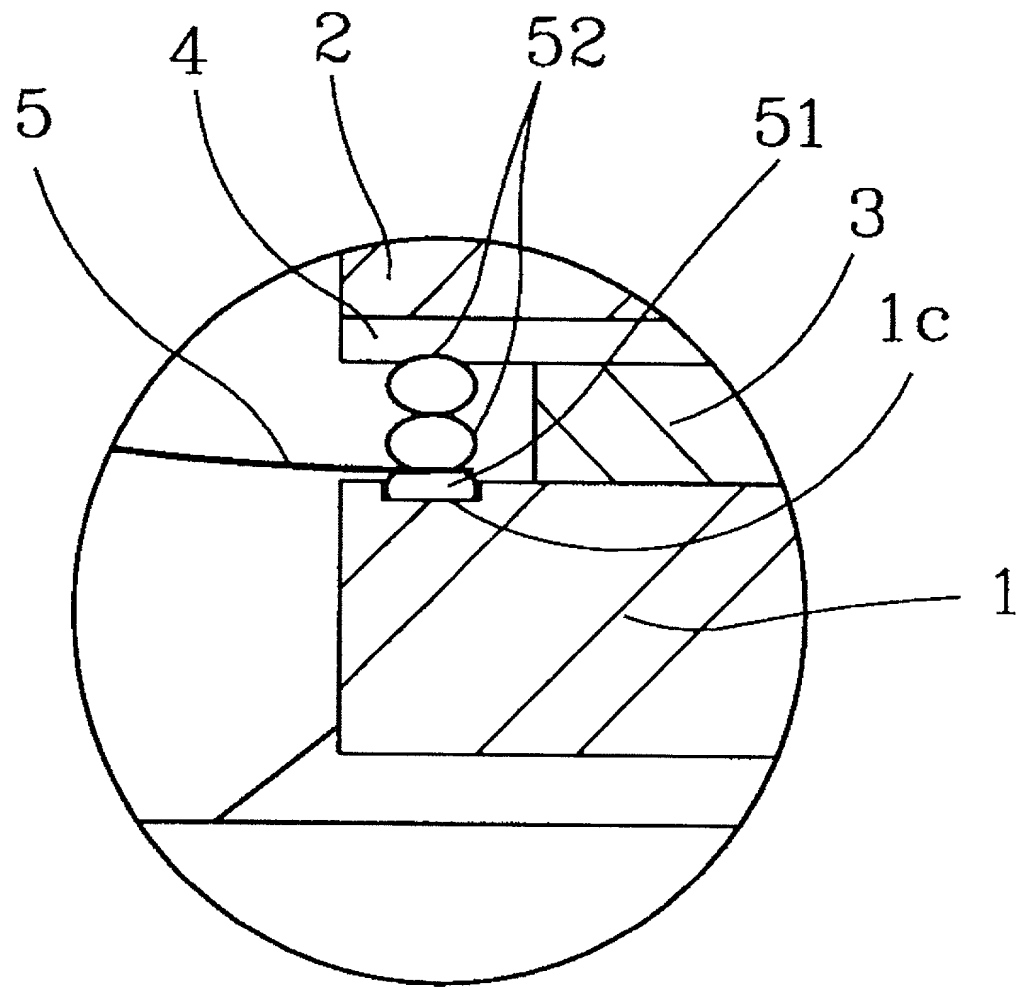


FIG. 3B

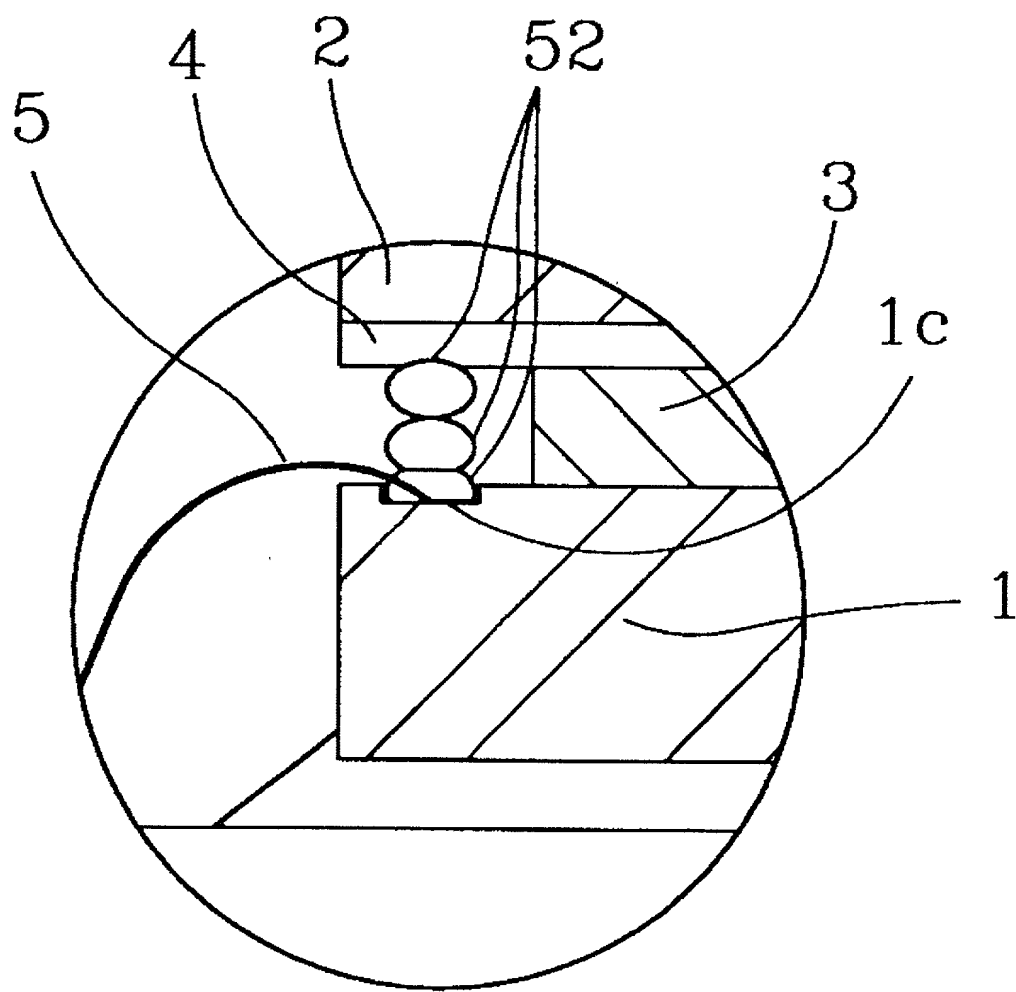


FIG. 4

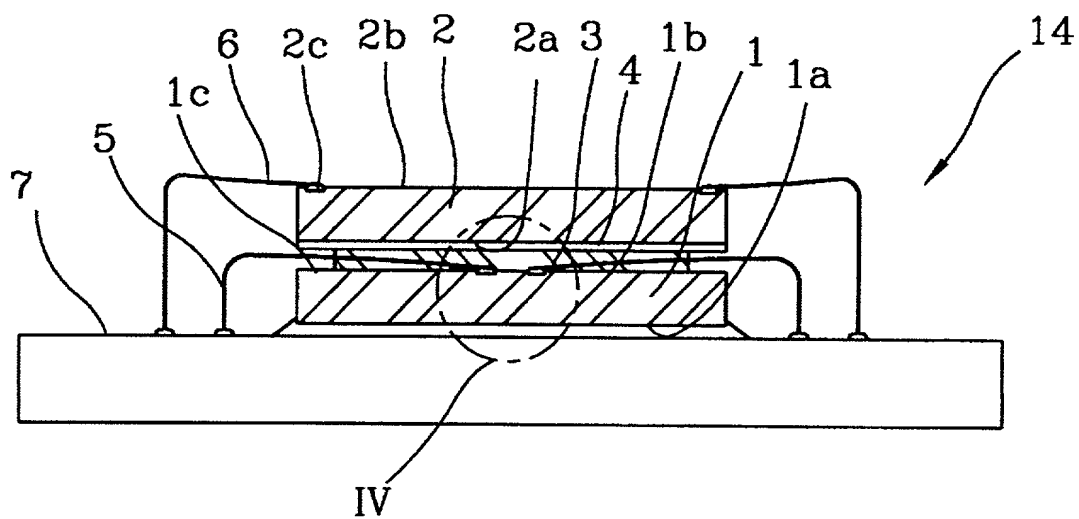


FIG. 4A

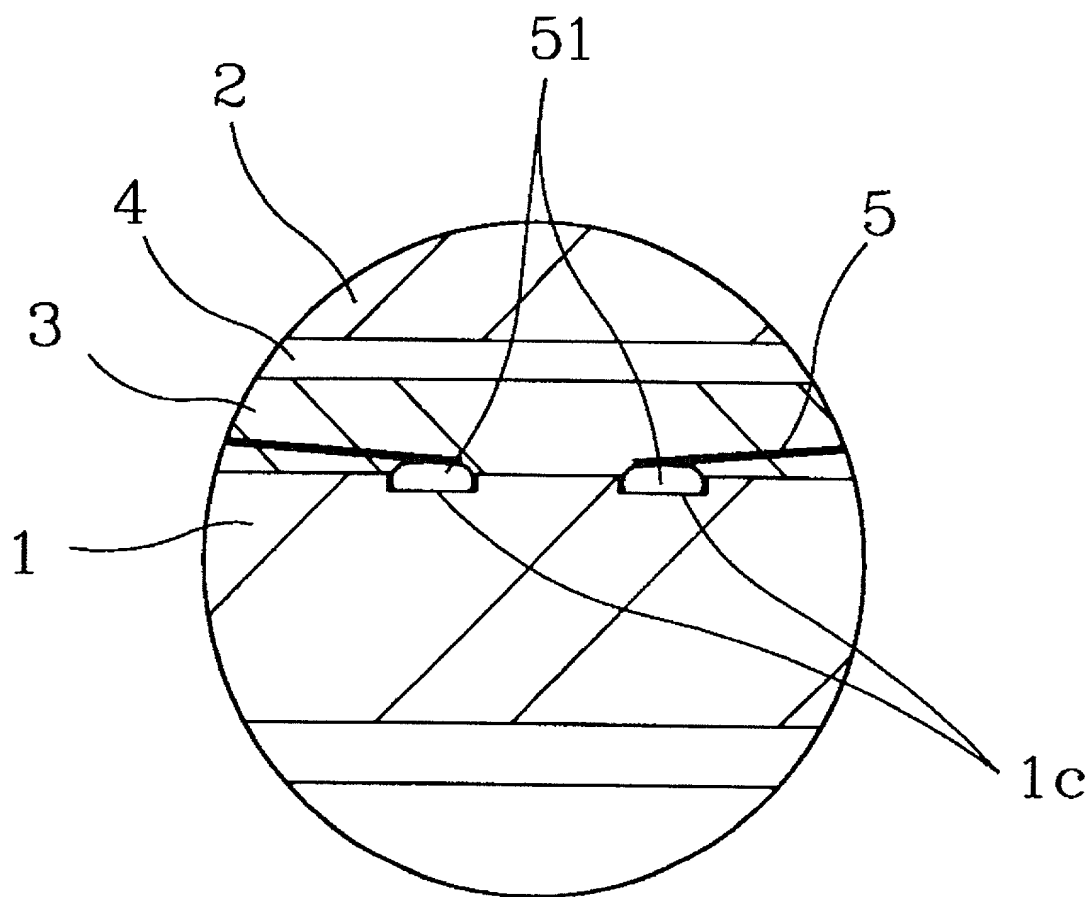


FIG. 5

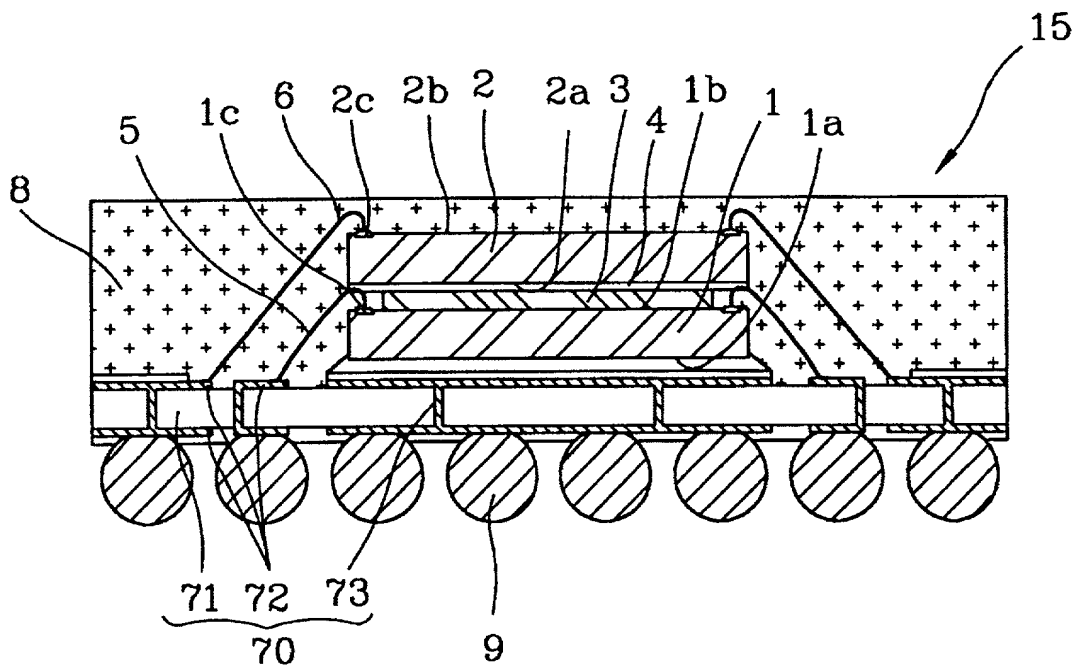


FIG. 6

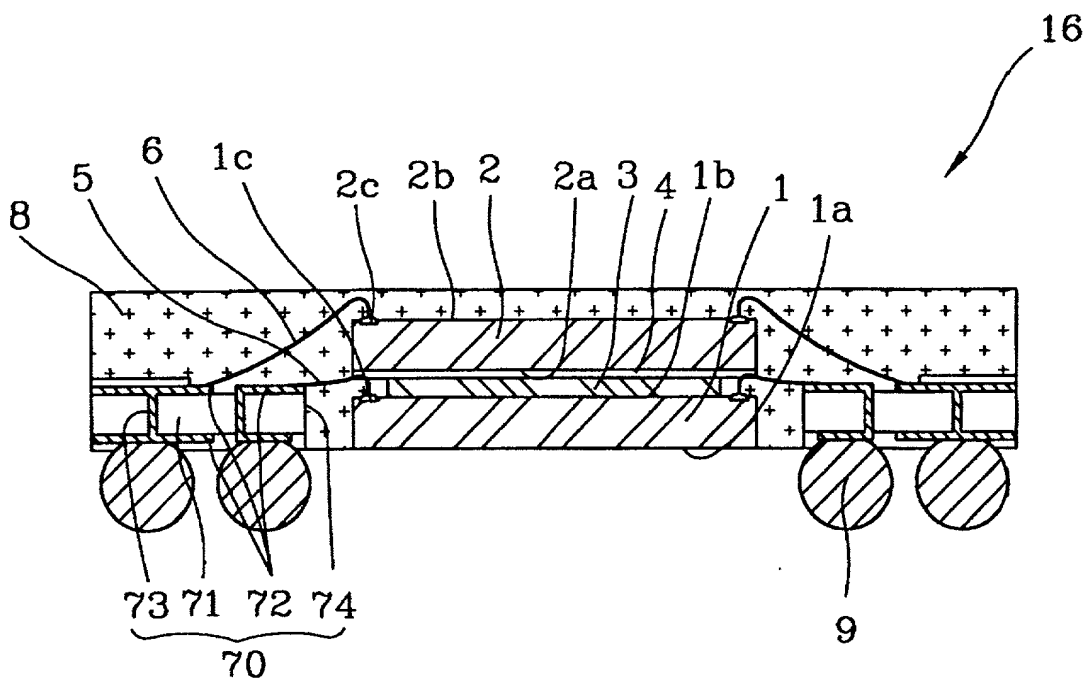
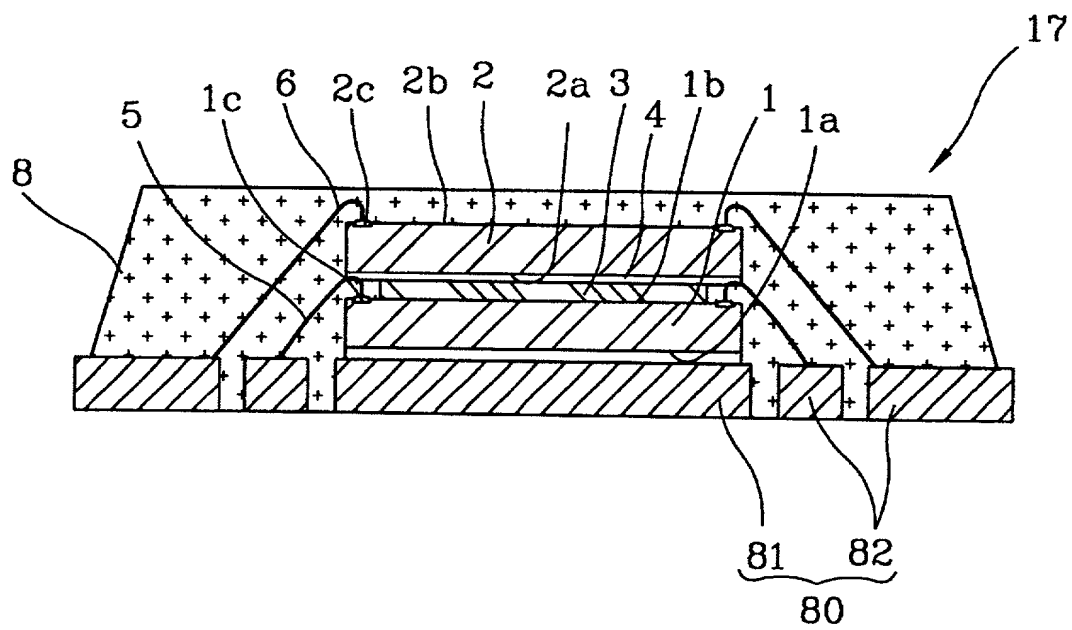


FIG. 7



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**DECLARATION FOR UTILITY OR
DESIGN
PATENT APPLICATION
(37 CFR 1.63)**

☒ Declaration Submitted with Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number W2K1070

First Named Inventor Oh et al.

COMPLETE IF KNOWN

Application Number

Filing Date

Art Unit

Examiner Name

As the below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**STACKING STRUCTURE OF SEMICONDUCTOR CHIPS AND SEMICONDUCTOR
PACKAGE USING IT**

(Title of the Invention)

the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YYYY) as United States Application Number or PCT International

Application Number and was amended on (MM/DD/YYYY) (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
2001-12326	Rep. of Korea	03/09/2001	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

[Page 1 of 2]

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NAME OF SOLE OR FIRST INVENTOR : ☐ A petition has been filed for this unsigned inventorGiven Name Kwang Seok
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or SurnameInventor's
Signature

Date 04/12/2001

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Country☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

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DECLARATION**ADDITIONAL INVENTOR(S)****Supplemental Sheet**Page 1 of 1**Name of Additional Joint Inventor, if any:**☐ A petition has been filed for this unsigned inventor

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Given
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Family Name
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Date 12/04/01

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DECLARATION — Supplemental Priority Data Sheet

	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403	2404	2405	2406	2407	2408	2409	2410	2411	2412	2413	2414	2415	2416	2417	2418	2419	2420	2421	2422	2
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